Listing of Claims:

1. (Currently Amended) An electrically erasable programmable read only memory (EEPROM) cell, comprising:

an isolation layer formed at a semiconductor substrate to define an active region;

a gate oxide layer formed on the semiconductor substrate;

a source region, a buried N+ region and a drain region formed at the active region and spaced apart from each other;

a cell depletion region formed at the active region between the buried N+ region and the drain region, the buried N+ region being in contact with the cell depletion region;

a first channel region between the source region and the buried N+ region;

a second channel region between the cell depletion region and the drain region;

a memory gate formed over the first channel region and the buried N+ region;

a selection gate formed over the second channel region;

a tunnel region formed through the gate oxide layer, wherein the tunnel region is self-aligned to the buried N+ region;

and a tunnel oxide layer formed between sidewalls of the tunnel region on the buried N+ region, wherein distances between the edges of the tunnel oxide layer and the buried N+ region are equidistant as a result of the tunnel region being self-aligned to the buried N+ region.

2. (Original) The EEPROM cell of claim 1, wherein the memory gate comprises:

a floating gate;

an inter-gate dielectric layer on the floating gate; and

a control gate electrode on the inter-gate dielectric layer.

3. (Original) The EEPROM cell of claim 1, wherein the selection gate comprises:

a lower selection gate;

an inter-gate dielectric layer on the lower selection gate; and

an upper selection gate on the inter-gate dielectric layer, the upper selection gate being electrically connected to the lower selection gate.

4. ~ 14. (Canceled)

15. (New) The EEPROM cell of claim 1, wherein the gate oxide layer has a thickness in a range of about 250 angstroms to about 350 angstroms.

16. (New) The EEPROM cell of claim 1, wherein the tunnel oxide layer is formed by thermal oxidation.

17. The EEPROM cell of claim 1, wherein the buried N+ region is wider than the tunnel region.